REMARKS

In response to the Office Action mailed on April 2, 2004, Applicant respectfully requests reconsideration. In this Amendment, claims 1 and 15 have been cancelled, and claims 2, 4, 5, 10-14, 16, 18-19 and 24-29 have been amended. In particular, previously dependent claims 5, 10-13, 19 and 24-27 have been re-written in independent form, and independent claims 28 and 29 have been amended to recite the use of a set speculation indicator instruction. Claims 2-14 and 16-29 are now pending. Applicant believe that the claims as presented are in condition for allowance. A notice to this affect is respectfully requested.

In the Office Action, claims 1-29 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,615,350 of Hesson et al. (hereinafter ("Hesson"). This rejection is respectfully traversed with respect to the claims as pending after the amendment herein.

Preliminarily, it is noted that in several instances the Office Action rejects claims based on Hesson as well as an assertion that a particular claim element is a "design choice". It is respectfully pointed out that the rejection of claims must be based on the prior art as reflected in the cited references and other evidence of record, and not on unsupported assertions. To the extent any claims are rejected on such a basis, it is respectfully urged that such rejections are not adequately supported and should therefore be withdrawn. In the traversals below, only the pertinent teachings of Hesson are discussed, because these are the only teachings of the prior art in evidence that are applied against the claims.

Hesson shows an apparatus for controlling out-of-order execution of load/store instructions that employs a "store barrier cache" to predict when a "store violation" is likely to occur. The store barrier cache is accessed in parallel with the fetching of an instruction, and if the virtual address of a store instruction matches an address in the store barrier cache, then a store barrier control bit is set. At the instruction issue stage, if the store barrier control bit is set, then load instructions that follow the store instruction in program order are prevented from

issuing. The store barrier control bit is subsequently cleared when the store instruction has successfully executed.

Hesson does not show any programmed control of the store barrier bit, i.e., it is not possible for instructions of an executing program to directly manipulate the value of the store barrier bit and thereby control whether out-of-order execution is permitted. Rather, the store barrier control bit is automatically deasserted by the processor hardware, specifically when two successive writebacks of store instruction data exhibit no violation condition.

Additionally, Hesson is seen to focus only on the problem of avoiding load-after-store hazards in a single processor. Hesson does not show a multi-processing environment nor any mechanism for controlling out-of-order execution so as to avoid the kinds of hazards that arise in such multi-access environments.

Claim 5 recites a method of controlling speculative execution of instructions in a processor operating in a uniaccess execution environment. The value of a speculation indicator is set to indicate that speculative execution of load instructions is allowed, and based on this value speculative execution of instructions is allowed in the processor. As part of allowing speculative instruction execution, the method includes deactivating a multiaccess speculative execution correction mechanism that exists in the computerized device. As described in the specification, a processor according to claim 5 includes a multiaccess speculative execution correction mechanism in order to detect and correct for situations in which speculative execution has created a hazard with respect to correct execution of interprocess communication or synchronization. Because the processor is executing in a uniaccess execution environment, there is no risk of such situations occurring. Thus the speculation indicator is used to deactivate the multiaccess speculative execution correction mechanism.

It is respectfully urged that claim 5 is not anticipated by Hesson, because Hesson fails to teach or suggest all the elements thereof. In particular, Hesson does not show a method of controlling speculative execution of instructions in a processor operating in a uniaccess execution environment that includes

deactivating a multiaccess speculative execution correction mechanism. Hesson does not show the use of a processor in a multiaccess manner, nor any correction mechanism for correcting for multiaccess speculative execution. Therefore, Hesson cannot show any manner of deactivating such a correction mechanism, specifically not as part of allowing speculative execution based on the value of a speculation indicator. Because Hesson lacks these features of claim 5, it is respectfully urged that Hesson does not anticipate claim 5 under 35 U.S.C. § 102(b).

Claim 10 recites a method for controlling speculative execution of instructions on a processor in a multiaccess execution environment, in which the value of a speculation indicator is set to indicate that speculative execution of load instructions is allowed if the process containing the instructions does not contain a shared memory condition.

It is respectfully urged that claim 10 is not anticipated by Hesson, because Hesson fails to teach or suggest all the elements thereof. In particular, Hesson does not show a method of controlling speculative execution of instructions in a processor in which the value of a speculation indicator is set to indicate that speculative execution of load instructions is allowed if the process containing the instructions does not contain a shared memory condition. As mentioned above, Hesson does not show the use of a processor in a multi-processing or multi-access environment – the setting of the store barrier control bit in Hesson is necessarily without regard to whether there is any shared memory condition. Therefore, Hesson cannot show a process that contains a shared memory condition. Because Hesson lacks this feature of claim 10, it is respectfully urged that Hesson does not anticipate claim 10 under 35 U.S.C. § 102(b).

Claim 11 recites a method for controlling speculative execution of instructions in which the value of a speculation indicator is determined by consulting the speculation indicator in a processor control register associated with the processor in the computerized device. By "processor control register" is meant a register that provides control information for the processor and that is

visible and writeable by software executing on the processor (e.g. by performing a SET SI instruction as described in the application). As described in the specification, the use of a processor control register gives direct control of the speculation indicator to an operating system or other program executing on the processor.

It is respectfully urged that claim 11 is not anticipated by Hesson, because Hesson fails to teach or suggest all the elements thereof. In particular, Hesson does not show a method of controlling speculative execution of instructions in a processor in which the value of a speculation indicator is determined by consulting the speculation indicator in a processor control register associated with the processor. In Hesson, the store barrier control bit does not reside in a processor control register, but rather is an output of a "rename unit" 12 that is operating in response to the detection of a store violation condition in the manner summarized above. The value of the store barrier control bit cannot be set by a software instruction such as a "SET SI" instruction, and in fact Hesson does not teach or suggest any such instruction. Because Hesson lacks this feature of claim 10, it is respectfully urged that Hesson does not anticipate claim 10 under 35 U.S.C. § 102(b).

It will be appreciated that the above comments pertaining to claim 11 are pertinent to claims 12 and 13 as well. Claim 13 recites the use of a set speculation indicator instruction, which is nowhere shown in Hesson. Claim 12 recites the use of a page table entry, which is another software-writeable item, to contain the speculation indicator. It is clear that Hesson does not teach the use of any such structure for the store barrier control bit. Accordingly, it is believed that neither claim 12 nor clam 13 is anticipated by Hesson under 35 U.S.C. § 102(b).

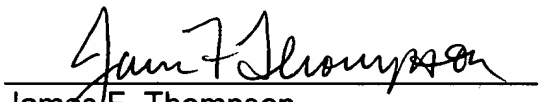
The remaining claims incorporate, either directly or indirectly, features appearing in claims 5 or 10-13 as discussed above, and therefore the above remarks are likewise applicable to the patentability of the remaining claims in view of Hesson.

In view of the foregoing, it is believed that all the claims of this application are allowable. Favorable action is respectfully requested. The Examiner is urged to telephone Applicants' attorney to resolve any issues that may be remaining.

If the U.S. Patent and Trademark Office deems a fee necessary, this fee may be charged to the account of the undersigned, Deposit Account No. 50-0901.

If the enclosed papers or fees are considered incomplete, the Patent Office is respectfully requested to contact the undersigned collect at (508) 366-9600, in Westborough, Massachusetts.

Respectfully submitted,



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